

Comp. Architecture

Sheet (1)

1	DRAM	SRAM
Application	is used in the - Fabrication of large memories Such as Main Memory (Hard disk...)	is used in building The Cache Memory & Sometimes in ROM because of its high Cost and Speed.
2		
Speed	Low	High
Size	Large	Small
Cost	Low	High
+ Construction	Capacitors + refreshment Circuits.	Transistors (Flip flops)

[3] The Types :

- ① PROM ② EPROM ③ EEPROM
- ④ Flash (memory)

[4]

EPROM

EEPROM

Flash (memory)

Erasable Programmed
ROM .

- Can be erased
as whole,
using ultra violet
rays .

Electrically
Erasable ROM .

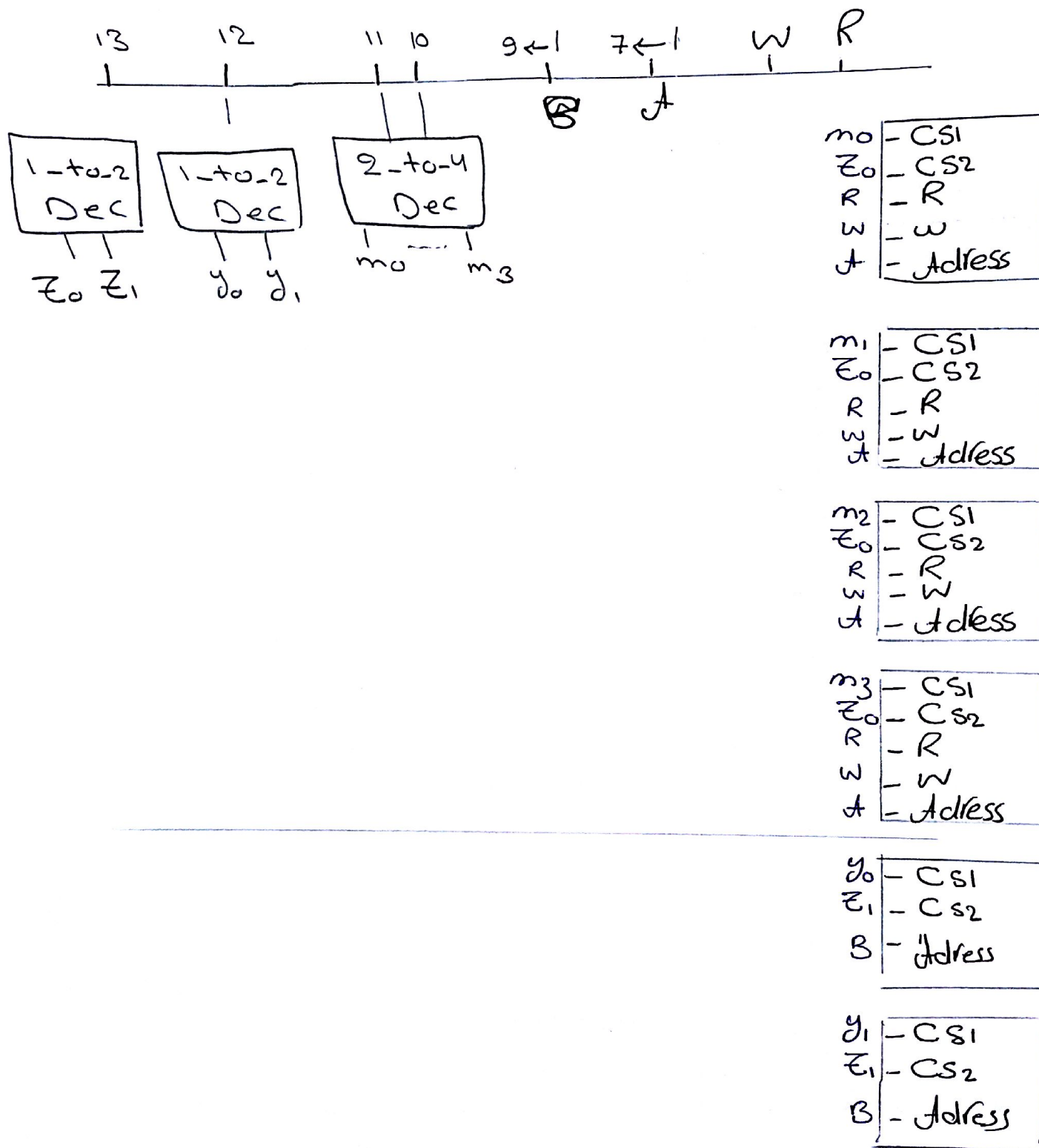
- is erased by
electric shots
is erased by
bit .

Flash memory .

- is erased by
electric shots
is erased by
block .

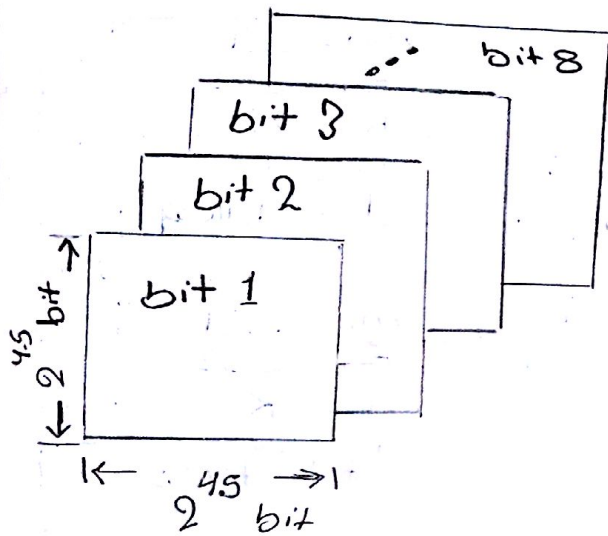
5 no. of RAM = $\frac{1024 \times 8}{256 \times 8} = 4 \text{ chips}$

no. of ROM = $\frac{2048 \times 8}{1024 \times 8} = 2 \text{ chips}$



6

RAM, ROM size = 512 bytes
= 512×8

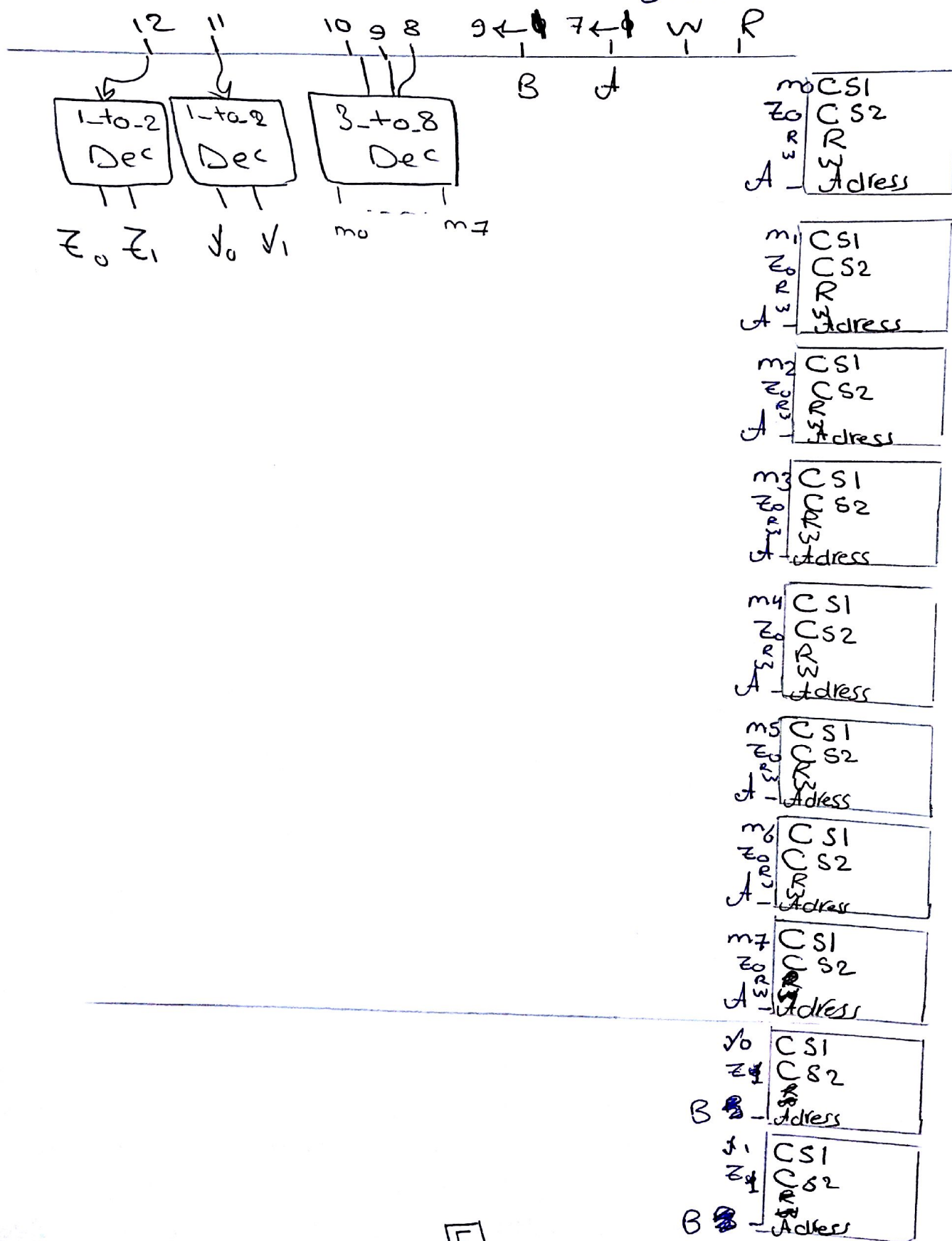


	0	1	2	3	4	5	6	7	9
0									2
1									
2									
511									

7

- no. of RAM chips = $\frac{1024 \times 8}{128 \times 8} = 8$ chips

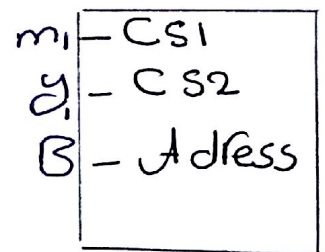
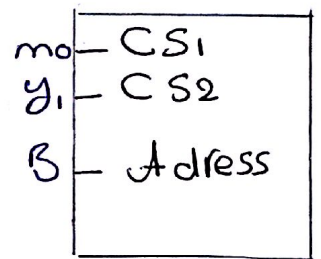
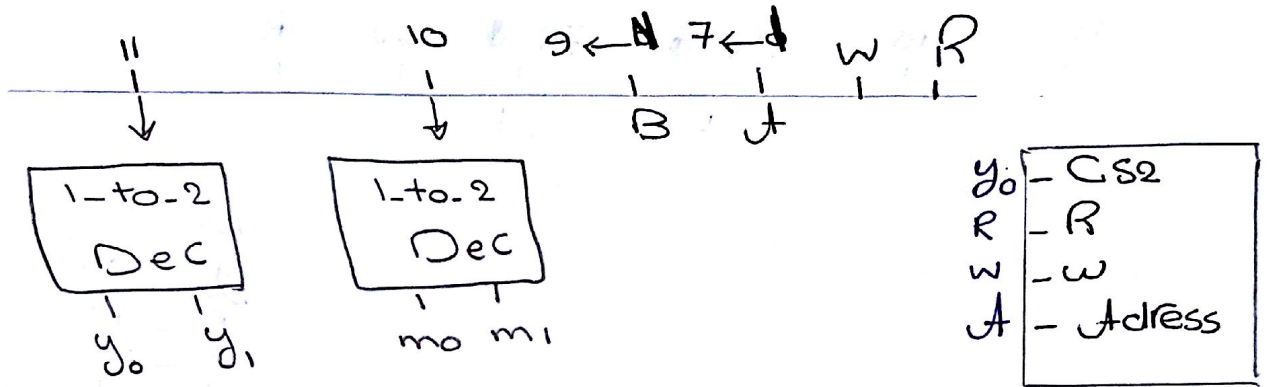
- no. of ROM chips = $\frac{1024 \times 8}{512 \times 8} = 2$ chips



5

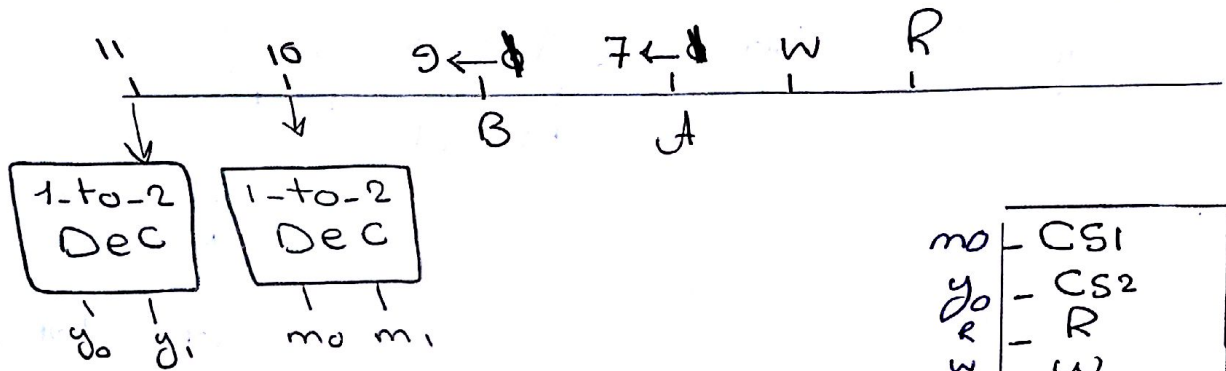
8] $\text{no. of RAM} = \frac{1024 \times 8}{1024 \times 8} = 1 \text{ Chip}$

$\text{no. of ROM} = \frac{1024 \times 8}{512 \times 8} = 2 \text{ Chip}$



9] no. of. ROM chips = $\frac{1024 \times 8}{512 \times 8} = 2 \text{ chips}$

no. of. RAM chips = $\frac{1024 \times 8}{1024 \times 8} = 1 \text{ chip}$



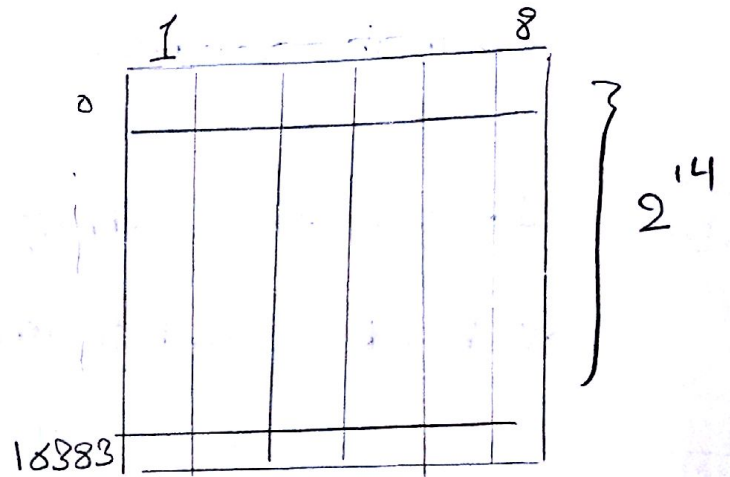
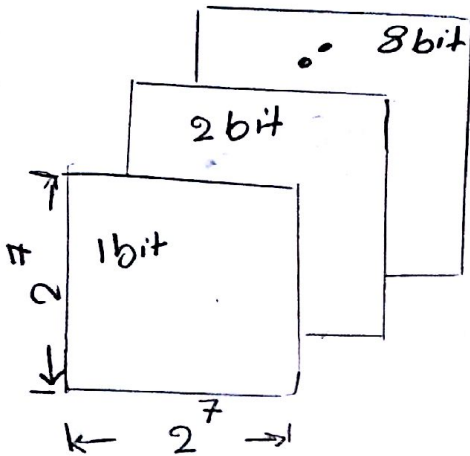
m_0	- CS1
y_0	- CS2
R	- R
w	- w
A	- Address

m_1	- CS1
y_1	- CS2
R	- R
w	- w
A	- Address

y_1	- CS2
B	- Address

Sheet (2)

1 no. of. lines = $\frac{128 \times 1024}{8} = 16384$ line
 $= 2^{14}$



2 no. of. words = $\frac{2^6 \times 2^{20}}{2^3} = 2^{32}$ word

ونكرر نفس الكلام نرسم مستطيل 8×2^{26} فمخولة اي blocks
 طول ضلعا 2^{13}

3 no. of. Caches/RAM = $\frac{2^{26} \text{ Byte}}{2^{17} \text{ Byte}} = 2^9 = 512$ Cache/RAM

[4] (Direct Mapping)

From [3] no. of Caches/RAM = 512

∴ There is 512 blocks Complete in each Set in The Cache.

[5] (Associative Mapping)

all blocks Complete in each set =

[6] (Set Associative Mapping)

- Set = 4 blocks (given)

∴ There is $512 \times 4 = \underline{2048}$ block Complete in each Set.

[7] 1/ FIFO means "First in First out"

∴ Associative and Set Associative is suitable for FIFO.

- The First data that went to Cache with is the first data to go out of it (Replaced).